What is claimed is:

1. A delay line unit of a delay locked loop (DLL) circuit, comprising:

a first delay line having a plurality of first unit delays, each first unit delay having a first delay;

a second delay line having a plurality of second unit delays, each second unit delay having a second delay; and

a third delay line having a plurality of third unit delays, each third unit delay having a third delay,

wherein the first delay is shorter than the second delay, and the second delay is shorter than the third delay.

2. The delay line unit as recited in claim 1, wherein the first, second and third delays are connected in series.

3. A delay locked loop (DLL) circuit used in a synchronous memory device, comprising:

a phase comparing unit for comparing a reference signal with a feedback signal and generating a comparison signal;

a delay controlling unit for generating a control signal in response to the comparison signal;

a delay line unit for delaying an internal clock signal in response to the control signal; and

a delay model for generating a feed back signal by delaying a clock signal,

wherein the delay line unit includes a plurality of delay lines, each delay line containing a plurality of unit delays having a different unit delay, respectively.

4. The DLL circuit as recited in claim 3, wherein the delay line unit includes:

a first delay line containing a plurality of first unit delays, each first unit delay having a first resolution;

a second delay line containing a plurality of second unit delays, each second unit delay having a second resolution; and

a third delay line containing a plurality of third unit delays, each third unit delay having a third resolution,

wherein the first, second and third delay lines are connected in series.

5. The DLL circuit as recited in claim 4, wherein the first resolution is lower than the second resolution, and the second resolution is lower than the third resolution.

6. A clock signal delay locking method in a delay locked loop (DLL) of a synchronous memory device, comprising the

steps of:

a) generating a comparison signal for comparing a reference signal with a feedback signal generated from a delay model;

b) generating a control signal in response to the comparison signal; and

c) delaying a clock signal by using a delay line unit containing a plurality of unit delays, each unit delay having a different resolution each other, in response to the control signal.

7. The clock signal delay locking method as recited in claim 6, wherein the step c) includes the steps of:

c1) delaying the clock signal through a first delay line containing a plurality of first unit delays, each having a first resolution;

c2), if a delay locking operation is not achieve in the step c1), delaying the clock signal through a second delay line containing a plurality of second unit delays, each having a second resolution, which is higher than the first resolution; and

c3), if a delay locking operation is not achieve in the step c2), delaying the clock signal through a third delay line containing a plurality of third unit delays, each having a

third resolution, which is higher than the second resolution.

8. The clock signal delay locking method as recited in claim 7, wherein the first, second and third delay lines are connected in series.